TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π-MOSV)

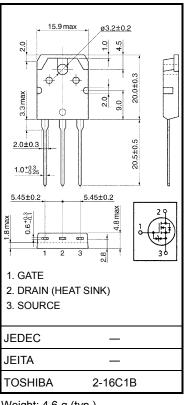
2SK2915

Chopper Regulator, DC–DC Converter and Motor Drive Applications

- Low drain-source ON resistance $RDS(ON) = 0.31 \Omega$ (typ.)
- High forward transfer admittance $: |Y_{fs}| = 15 \text{ S (typ.)}$
- Low leakage current $: I_{DSS} = 100 \ \mu A \ (max) \ (V_{DS} = 600 \ V)$
- Enhancement mode : $V_{th} = 2.0 \sim 4.0 V (V_{DS} = 10 V, I_D = 1 mA)$

Characteri	stics	Symbol	Rating	Unit	
Drain-source voltage		V _{DSS}	600	V	
Drain-gate voltage (R	_{GS} = 20 kΩ)	V _{DGR}	600	V	
Gate-source voltage		V _{GSS}	±30	V	
Drain current	DC (Note 1)	I _D	16	А	
	Pulse (Note 1)	I _{DP}	64	A	
Drain power dissipatio	n (Tc = 25°C)	PD	150	W	
Single pulse avalanch	e energy (Note 2)	E _{AS}	1026	mJ	
Avalanche current		I _{AR}	16	А	
Repetitive avalanche energy (Note 3)		E _{AR}	15	mJ	
Channel temperature		T _{ch}	150	°C	
Storage temperature r	ange	T _{stg}	-55~150	°C	

Absolute Maximum Ratings (Ta = 25°C)



Weight: 4.6 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	R _{th (ch-c)}	0.833	°C / W
Thermal resistance, channel to ambient	R _{th (ch−a)}	50	°C / W

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 7.01 mH, R_G = 25 Ω , I_{AR} = 16 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Please handle with caution.

Unit: mm

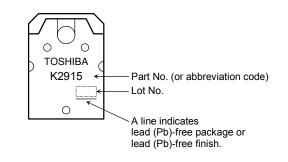
Electrical Characteristics (Ta = 25°C)

Chara	cteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GSS}	V _{GS} = ±25 V, V _{DS} = 0 V	_	—	±10	μA
Gate-source b	reakdown voltage	V (BR) GSS	I _G = ±10 μA, V _{DS} = 0 V	±30	_		V
Drain cut-off cu	rrent	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V		_	100	μA
Drain-source bi	reakdown voltage	V (BR) DSS	I _D = 10 mA, V _{GS} = 0 V	600	_		V
Gate threshold	voltage	V _{th}	V _{DS} = 10 V, I _D = 1 mA	2.0	—	4.0	V
Drain-source O	N resistance	R _{DS (ON)}	V _{GS} = 10 V, I _D = 8.0 A		0.31	0.4	Ω
Forward transfe	r admittance	Y _{fs}	V _{DS} = 10 V, I _D = 8.0 A	8.0	15.0		S
Input capacitance		C _{iss}		_	3520	_	
Reverse transfer capacitance		C _{rss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	_	20	_	pF
Output capacitance		C _{oss}			300	_	
Switching time	Rise time	tr	$V_{GS} \stackrel{10V}{}_{0V} \int_{U} \stackrel{I_{D}=8.0A}{}_{V_{OUT}} \\ \downarrow \qquad \downarrow$	_	50	_	ns
	Turn-on time	t _{on}		_	100	_	
	Fall time	t _f		_	60	_	
	Turn-off time	t _{off}	$v_{DD} \rightarrow 500 v$ Duty $\leq 1\%$, t _w = 10μ s	_	325	_	
Total gate charge (gate-source plus gate-drain)		Qg		_	80	_	
Gate-source charge		Q _{gs}	V _{DD} ≈ 400 V, V _{GS} = 10 V, I _D = 16 A		48	_	nC
Gate-drain ("miller") Charge		Q _{gd}			32	_	

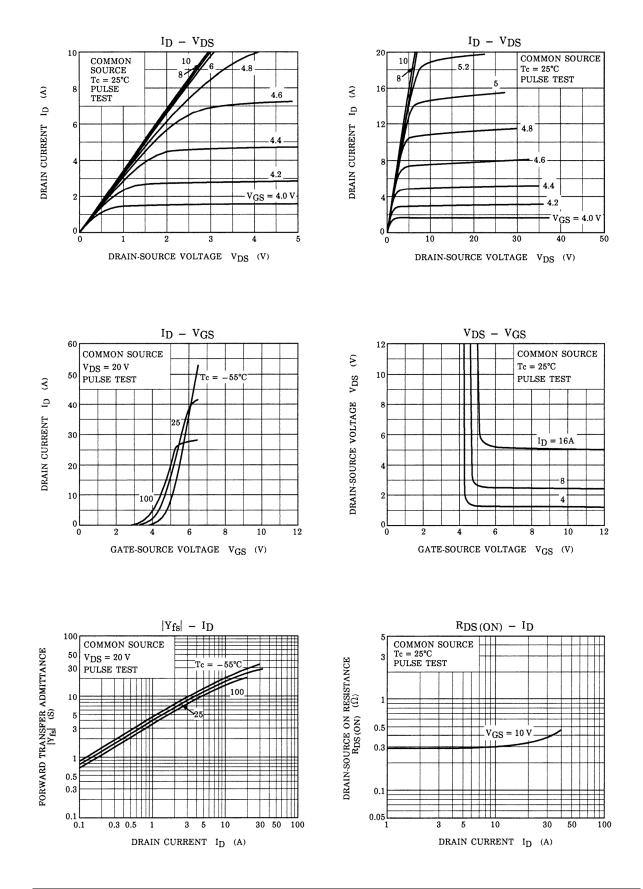
Source–Drain Ratings and Characteristics (Ta = 25°C)

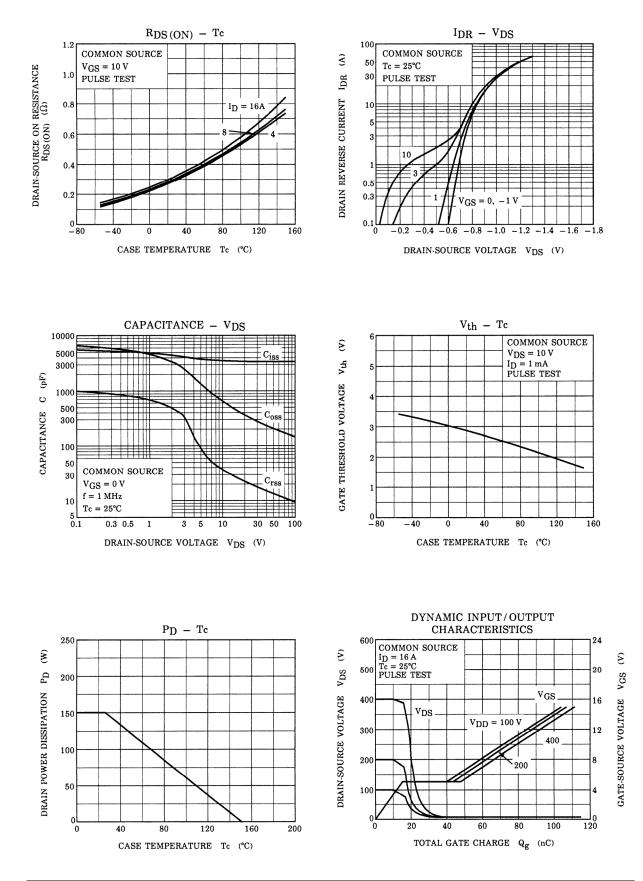
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1)	I _{DR}	—	_	_	16	А
Pulse drain reverse current (Note 1)	I _{DRP}	_	_	_	64	A
Forward voltage (diode)	V _{DSF}	I _{DR} = 16 A, V _{GS} = 0 V	_	_	-1.7	V
Reverse recovery time	t _{rr}	I _{DR} = 16 A, V _{GS} = 0 V dI _{DR} / dt = 100 A / μs		620		ns
Reverse recovery charge	Q _{rr}	dI _{DR} / dt = 100 A / μs	_	7.5	_	μC

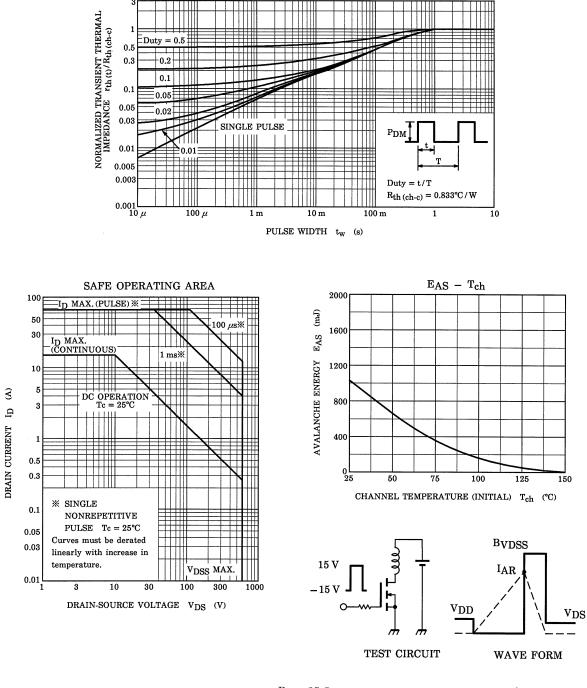
Marking



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 $r_{th} - t_w$

 $\begin{array}{ll} \mathrm{RG} = 25 \ \Omega \\ \mathrm{V_{DD}} = 90 \ \mathrm{V}, \ \mathrm{L} = 7.01 \ \mathrm{mH} \end{array} \qquad \mathrm{EAS} = \frac{1}{2} \cdot \mathrm{L} \cdot \mathrm{I}^2 \cdot \left(\frac{\mathrm{B} \mathrm{VDSS}}{\mathrm{B} \mathrm{VDSS} - \mathrm{V} \mathrm{DD}} \right) \\ \end{array}$

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